CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** A method of processing power mode instruction, comprising:

fetching and decoding a power mode instruction; and

executing the power mode instruction on a combination of a CPU clock source and a peripheral clock source, wherein the power mode instruction initiates a switch to a clock source configuration associated with a literal**[.]**

2. (Original) The method according to claim 1, wherein the power mode instruction is a first power mode instruction.

3. (Original) The method according to claim 2, wherein the clock source configuration for the first power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a primary oscillator.

4. (Original) The method according to claim 1, wherein the power mode instruction is a second power mode instruction.

5. (Original) The method according to claim 4, wherein the clock source configuration for the second power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a low power internal RC.

6. (Original) The method according to claim 1, wherein the power mode instruction is a third power mode instruction.

7. (Original) The method according to claim 6, wherein the clock source configuration for the second power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a secondary oscillator.

8. (Original) The method according to claim 1, wherein the power mode instruction is a fourth power mode instruction.

9. (Original) The method according to claim 8, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and the peripheral clock source.

10. (Original) The method according to claim 1, wherein the power mode instruction is a fifth power mode instruction.

11. (Original) The method according to claim 10, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and deriving the peripheral clock source from a low power internal RC.

12. (Original) The method according to claim 1, wherein the power mode instruction is a sixth power mode instruction.

13. (Original) The method according to claim 1, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and deriving the peripheral clock source from a secondary oscillator.

14. (Original) The method according to claim 1, further comprising:
detecting that an interrupt condition has occurred.

15. (Original) The method according to claim 14, further comprising:

loading an instruction immediately following the power mode instruction into an instruction register for execution.

16. (Original) The method according to claim 14, further comprising:

loading the first instruction in an interrupt service routine for the interrupt into an instruction register for execution.

17. (Original) The method according to claim 14, further comprising:

determining whether to service an interrupt associated with the interrupt condition based on CPU priority.

18. **(Currently Amended)** A processor for performing a power mode instruction, comprising:

a program memory for storing instructions including a shadow register array control instruction;

a program counter for identifying current instructions for processing; and

a clock transition logic for executing the power mode instruction on a combination of a CPU clock source and a peripheral clock source, wherein the power mode instruction initiates a switch to a clock source configuration associated with a literal**[.]**

19. (Original) The processor according to claim 18, wherein the power mode instruction is a first power mode instruction.

20. (Original) The processor according to claim 19, wherein the clock source configuration for the first power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a primary oscillator.

21. (Original) The processor according to claim 18, wherein the power mode instruction is a second power mode instruction.

22. (Original) The processor according to claim 21, wherein the clock source configuration for the second power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a low power internal RC.

23. (Original) The processor according to claim 18, wherein the power mode instruction is a third power mode instruction.

24. (Original) The processor according to claim 23, wherein the clock source configuration for the second power mode instruction corresponds to the CPU clock source and the peripheral clock source derived from a secondary oscillator.

25. (Original) The processor according to claim 18, wherein the power mode instruction is a fourth power mode instruction.

26. (Original) The processor according to claim 25, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and the peripheral clock source.

27. (Original) The processor according to claim 18, wherein the power mode instruction is a fifth power mode instruction.

28. (Original) The processor according to claim 27, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and deriving the peripheral clock source from a low power internal RC.

29. (Original) The processor according to claim 18, wherein the power mode instruction is a sixth power mode instruction.

30. (Original) The processor according to claim 29, wherein the clock source configuration for the second power mode instruction corresponds to disabling the CPU clock source and deriving the peripheral clock source from a secondary oscillator.

31. (Original) The processor according to claim 18, further comprising:

interrupt logic for detecting that an interrupt condition has occurred.

32. (Original) The processor according to claim 31, further comprising:

an instruction register for loading an instruction immediately following the power mode instruction into an instruction register for execution interrupt service routine (ISR) for an interrupt servicing the interrupt condition.

33. (Original) The processor according to claim 31, further comprising:

an instruction register for loading the first instruction in an interrupt service routine for the interrupt into an instruction register for execution.